showing the desired amendments to the originally filed Claim 1, and correcting the unintentional inconsistencies in the previously presented claim. Amended Claim 1 as presently presented also contains additional amendments in light of the Examiner's additional analysis.

Remarks

In the Office Action, the Examiner noted that Claims 1-36 are pending in the application, and that Claims 1-36 are rejected. By this amendment, Claims 1 and 3 have been amended. Thus, Claims 1-36 are pending in the application. The Examiner's rejections are traversed below.

Analysis of Claim Elements and Functional Limitations

Examiner's insightful revision of the claim analysis improves upon the analysis presented by the Applicants. However, Applicants respectfully submit the following further revision of the claim analysis to facilitate examination of the present application.

The elements "a memory" and "a computer system memory" are separate and distinct elements. Although similar, Applicants do not believe that any ambiguity is introduced thereby. The element "a memory" generally is used to describe the logical representation of a memory cell and/or device being designed and tested in an automated manner utilizing a computer system. The element "a computer system memory" generally is used to describe the physical location for storing the logical representation in the computer system.

Applicants' continue to maintain that "a memory" is an element of the claim. Although "a memory" is introduced in the preamble, the element is also present in the body of the claim and therefore is properly an element of the claim.

Applicants also assert that "a memory" is logically represented by a plurality of models. First, "a memory" is logically represented by "a simulation model" of "said memory". A "simplified behavioral model" of "said memory" is generated by re-describing "said memory" based upon "said simulation model" of "said memory" utilizing "a behavioral hardware descriptive language". The "simplified behavioral model" of "said memory" is translated into "said structural model" of "said memory".

The Examiner has also re-characterized the functional limitations of "translating", "automatically", and "under control" as a collective functional limitation. Although Applicants characterize each as separately required, the Examiner implicitly acknowledges that each are required to satisfy the collective functional limitation. Similarly, the Examiner has also re-characterized the functional limitations of "generating" and "re-describing" as a collective functional limitation. Based upon the analysis presented by Examiner, there does not appear to be a significant difference as to whether each are properly characterized as individual functional limitations or as a collective functional limitation. Therefore in the interest of expediting prosecution, the Applicants will defer to the Examiner's interpretation, unless subsequent analysis of prior

art by the Examiner necessitates revisiting the distinction between an individual or a collective functional limitation.

Rejections Under 35 USC 102(b) and 103

Claim 1 stands rejected under 35 USC 103, as being rendered obvious by Beausang US Patent 5,696,771 in view of legal precedent (MPEP 2144.04(II)). The Examiner has correctly noted that Beausang does not disclose:

> generating a simplified behavioral model of said memory by re-describing said memory with a predefined proper subset of said behavioral hardware description language.

However, the Examiner asserts that omission of an element and it function is obvious if the function of the element is not desired. The legal precedent provided cited in MPEP 2144.04(II) and relied upon by the Examiner is distinguishable from the invention as claimed by Claim 1. According to the legal precedent, the omission of the particular element and it function is taught and/or suggested by the reference. For example, Ex parte Wu, the claims were **directed to** a method for inhibiting corrosion in an environment not containing fresh water. The references taught or suggested additional of elements to inhibit corrosion in a fresh water environment. Hence, the omitted element and function was directly related to the claimed invention and thus was inherently and/or expressly taught and/or suggested.

If leaving out an element alone without any suggestion or motivation to do so rendered an application obvious, than only inventions that provide a solution to a problem which is more complicated than the prior solution would be

patenable. Clearly, a less complicated solution to a given problem should also be patenable, unless the prior art method at least provides a motivation or suggest the removal of the particular element at issue.

Claim 1 of the present invention is directed to a method of constructing a structural model for use in automatic test pattern generation. The omission of a predefined proper subset of said behavioral hardware from a simplified simulation model is not directly related to constructing a structural model for use in automatic test pattern generation. For example, the omission of timing and/or layout information does not in and of itself teach, suggest or provide the motivation to modify a simulation model to create a structural model for use in automatic test pattern generation. Furthermore, there is no suggestion to selectively omit timing and/or layout information as opposed to one or more of the other categories of information contained in the simulation model in order to create a structural model for use in automatic test pattern generation.

The rejection does not indicate a prior art reference which suggests and/or teaches the exclusion of the predefined proper subset of the behavioral hardware from the simplified model, as taught and claimed in Claim 1. Hence, the rejection fails to make a prima facie case of obviousness.

The rejection also alleges that Beausang discloses:

> translating, automatically and under control of a computer system, said simplified behavioral model into said structural

model of said memory, wherein said structural model comprises a plurality of ATPG memory primitives.

However, Beausang clearly does not teach or suggest translating a simplified behavioral model into a structural model. At col. 14 lines 39-42, the logical primitive relates to the technology independent netlist 620 (See also Figure 8). The technology independent netlist 620 containing the logical primitive is not the same netlist applied to the "ATPG AND FORMAT" at Figure 8 element 655. Furthermore, as described at col. 14 line 44 through col. 16 line 23, the technology independent netlist 620 is operated upon resulting in a non-scannable netlist 630; the non-scannable netlist 630 is operated upon resulting in a scannable netlist 650; the scannable netlist 650 is operated upon resulting in a system level scannable netlist 653. The system level scannable netlist 653 is then input to the automatic test pattern generation procedure. If there is any equivalence between the passage in Beausang cited and the present invention, Beausang teaches a method comprising at least two intermediate steps as opposed to the single intermediate step of generating a simplified behavioral model.

Furthermore, Applicants respectfully assert that Beausang does not teach or suggest how to translate a simplified behavioral model to a corresponding structural model. In addition, generating the simplified behavioral model, which is translated into a corresponding structural model, is not disclosed by legal precedent. Therefore, withdrawal of this rejection is respectfully requested.

Claims 2 and 3 stand rejected under 35 USC 103, as being rendered obvious by Beausang US Patent 5,696,771 in view of legal precedent (MPEP 2144.04(II)) and Cheng. Neither Beausang nor Cheng teach or suggest creating a structural model from a corresponding simulation model.

The Examiner correctly notes that Beausang does not disclose generating a structural model based upon a simplified behavioral model, which excludes timing and/or layout information of a corresponding simulation model.

Furthermore, Cheng actually teaches away from the present invention. Cheng teaches that circuit delays are neglected during test pattern generation (page 406, last line through page 407, line 11). Hence, Cheng implies that the structural models utilized to generate test patterns contain timing and/or layout information. If the structural models did not contain timing and/or layout information, than there would be no circuit delays to be ignored Ignoring delays is not necessarily equivalent to excluding timing and/or layout information. Furthermore, if ignoring delays is equivalent to excluding timing and/or layout information, than Cheng would effectively teach that all state changes during application of one or more test vectors happen instantaneously and/or simultaneously. Applicants assert that a more reasonable interpretation is that timing and/or layout information is not excluded according to Cheng. Instead Cheng suggests that timing and/or layout information is utilized, but delay resulting from different signal propagation paths may be ignored altogether or at least during a first iteration.

Thus, neither Beausang, legal precedent nor Cheng teach, suggest or provide the motivation to exclude timing and/or physical layout information from the simplified behavioral model utilized to generate the corresponding structural model. Withdrawal of the rejection of Claims 2 and 3 is therefore respectfully requested.

Claims 4-8 stand rejected under 35 USC 103, as anticipated by Beausang US Patent 5,696,771. The rejection alleges that Beausang disclosed a plurality of ATPG memory primitives each represent a functionality at col. 14, line 40. However, the referenced passage actually teaches that a netlist is composed of logical primitives. Thus, Beausang does not teach what a logical primitive represents.

The Applicants are not claiming all logical primitives as a collective whole. Applicants are claiming that an ATPG memory primitive according to the present invention represents a functionality. In addition, Applicants are claiming that an ATPG memory primitive according to the present invention comprises a plurality of other primitives (e.g., memory primitive, address bus primitive, data bus primitive, read port primitive, etc.).

Beausang does not teach and/or suggest what a logical primitive comprises. Furthermore, Beausang does not teach that an ATPG memory primitive represents a functionality and/or a plurality of other primitives coupled and interacting in a particular configuration. Withdrawal of the rejection of Claims 4-8 is therefore respectfully requested.

Claims 9-12 stand rejected under 35 USC 102(b), as being anticipated by Beausang US Patent 5,696,771. Applicants respectfully submit that Claims 9-12, depend from patentable independent Claim 1, and incorporate all the limitation thereof. Thus, Claims 4-12, are also patentable over Beausang. Withdrawal of the rejection of Claims 9-12 is therefore respectfully requested.

Claims 13-24 and 25-36 stand rejected for the same reasons as Claims 1-12. Applicants respectfully submit that Claims 13-24 and 25-36 are patentable for the same reasons advanced with respect to Claims 1-12 Withdrawal of the rejection of Claims 13-24 and 25-36 is therefore respectfully requested.

Conclusion

For all the reasons advanced above, Applicants respectfully submits that the application is in condition for allowance and that action is earnestly solicited. The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

The Commissioner is hereby authorized to charge any additional fees, which may be required for this amendment, or credit any overpayment, to Deposit Account 23-0085.

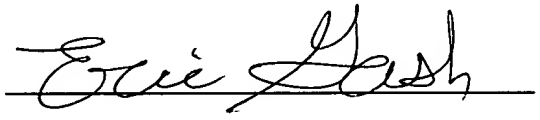
In the event that an extension of time is required, or may be required in addition to that requested in a petition for an extension of time, the

Commissioner is requested to grant a petition for that extension of time which is required to make this response timely and is hereby authorized to charge any fee for such an extension of time or credit my overpayment for an extension of time to Deposit Account 23-0085.

Respectfully submitted,

WAGNER, MURABITO & HAO, LLP

Dated: January 23, 2003



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VERSION WITH MARKING TO SHOW CHANGES MADE

In the claims

1. (Twice Amended) A method of constructing a structural model ~~for~~ of a memory for use in an ATPG (Automatic Test Pattern Generation), said method comprising the steps of:

accessing a simulation model of said memory, from a simulation library stored in ~~memory of~~ a computer system memory, wherein said simulation model is described in a behavioral hardware description language;

generating a simplified behavioral model of said memory by re-describing said memory with a predefined proper subset of said behavioral hardware description language; ~~and~~

~~under computer control, automatically~~ translating, automatically and under control of a computer system, said simplified behavioral model of said memory into said structural model of said memory, ~~and storing said structural model in said memory~~ wherein said structural model comprises a plurality of ATPG memory primitives; and

storing said structural model in said computer system memory.

3. (Amended) A method as recited in Claim 2 further wherein said simplified behavioral model excludes physical layout information contained in said simulation model of said memory.